What is claimed is:

1. A semiconductor integrated circuit having a plurality of CMOS inverters connected in an odd number of stages and a ring oscillator circuit for feeding a final-stage output signal of a final-stage CMOS inverter back to an input end of a first-stage CMOS inverter thereby causing self-oscillation, the semiconductor integrated circuit wherein:

the first-stage CMOS inverter comprises

a transistor series circuit including PMOS and NMOS transistors connected between a power voltage terminal and a reference voltage terminal, and

a delay circuit for delaying a first-stage output signal of the first-stage CMOS inverter; and

the delay circuit comprises

a capacitor coupled between an output node of the first-stage CMOS inverter and the reference voltage terminal, and

a resistance parallel circuit inserted and coupled on a current passage of the transistor series circuit at between the output node and the reference voltage terminal;

the resistance parallel circuit being configured by a parallel connection of a plurality of resistance elements different in resistance-value temperature characteristic.

2. A semiconductor integrated circuit according to claim 1, wherein the plurality of resistance elements different in resistance-value temperature characteristic are a first resistance element having a resistance value decreasing with

increasing temperature and a second resistance element having a resistance value nondependent upon temperature.

3. A semiconductor integrated circuit having a plurality of CMOS inverters connected in an odd number of stages and a ring oscillator circuit for feeding a final-stage output signal of a final-stage CMOS inverter back to an input end of a first-stage CMOS inverter thereby causing self-oscillation, the semiconductor integrated circuit comprising:

the first-stage CMOS inverter having first and second sub-CMOS inverters to which the final-stage output signal is to be fed back;

a second-stage CMOS inverter being configured by a logic gate having first and second input terminals to which first and second first-stage output signals of the first and second sub-CMOS inverters are to be respectively supplied;

the first sub-CMOS inverter having a first transistor series circuit including a first PMOS transistor and first NMOS transistor coupled between a power voltage terminal and a reference voltage terminal, and a first delay circuit for delaying the first-stage output signal;

the second sub-CMOS inverter having a second transistor series circuit including a second PMOS transistor and second NMOS transistor coupled between the power voltage terminal and the reference voltage terminal, and a second delay circuit for delaying the second-stage output signal;

the first delay circuit having a first capacitor

coupled between a first output node of the first sub-CMOS inverter and the reference voltage terminal and a first resistance element inserted and coupled on a current passage of the first transistor series circuit at between the first output node and the reference voltage terminal and having a resistance value decreasing with increasing temperature; and

the second delay circuit having a second capacitor coupled between a second output node of the second sub-CMOS inverter and the reference voltage terminal and a second resistance element inserted and coupled on a current passage of the second transistor series circuit at between the second output node and the reference voltage terminal and having a resistance value nondependent upon temperature.

4. A semiconductor integrated circuit, comprising:

an oscillation period determining device including first and second oscillation period determining circuits, to output as a final output an output signal shorter in oscillation period of two output signals outputted by the two oscillation period determining circuits;

the first oscillation period determining circuit having a first oscillator circuit;

the first oscillator circuit having a plurality of CMOS inverters connected in an odd number of stages, so that an output signal of a final-stage CMOS inverter can be fed back to an input end of a first-stage CMOS inverter thereby causing self-oscillation;

the first-stage CMOS inverter having a first

transistor series circuit including a first PMOS transistor and first NMOS transistor coupled between a power voltage terminal and a reference voltage terminal, and a first delay circuit for delaying the first-stage output signal of the first-stage CMOS inverter;

the first delay circuit having a first capacitor coupled between a first output node of the first sub-CMOS inverter and the reference voltage terminal and a first resistance element inserted and coupled on a current passage of the first transistor series circuit at between the first output node and the reference voltage terminal and having a resistance value decreasing with increasing temperature; and

the second oscillation period determining circuit outputting an output signal having an oscillation period nondependent upon temperature.

5. A semiconductor integrated circuit according to claim 4, wherein the first oscillation period determining circuit has a first frequency divider circuit for dividing a frequency of an output signal of the first oscillator circuit to adjust an oscillation period, the first frequency divider circuit having an adjuster for changing a frequency dividing period in order to divide a frequency of an output signal of the first oscillator circuit.

6. A semiconductor integrated circuit according to claim 4 or 5, wherein the second oscillation period determining circuit is configured by a second oscillator circuit and a second frequency divider circuit; the second oscillator

circuit having a plurality of CMOS inverters connected in an odd number of stages so that an output signal of the final-stage CMOS inverter can be fed back to an input end of the first-stage CMOS inverter thereby causing self-oscillation; the first-stage CMOS inverter of the second oscillator circuit having a second transistor series circuit including a second PMOS transistor and second NMOS transistor coupled between the power voltage terminal and the reference voltage terminal, and a second delay circuit for delaying a first-stage output signal of the first-stage CMOS inverter of the second oscillator circuit; the second delay circuit having a second capacitor coupled between a second output node of the second sub-CMOS inverter and the reference voltage terminal, and a second resistance element inserted and coupled on a current passage of the second transistor series circuit at between the second output node and the reference voltage terminal and having a resistance value nondependent upon temperature.